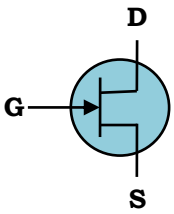
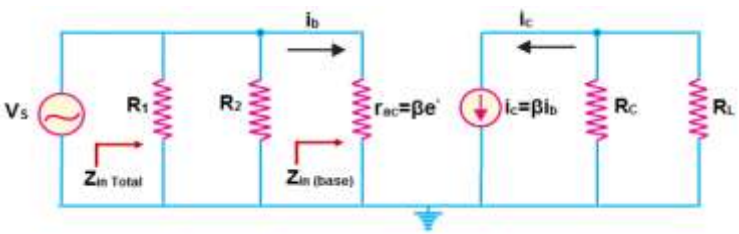
GOVERNMENT OF KARNATAKA
DEPARTMENT OF PRE - UNIVERSITY EDUCATION
II YEAR PUC ANNUAL EXAMINATION APRIL/MAY -2022
SCHEME OF VALUATION

Subject code:40 **Subject: ELECTRONICS**

Qn. No.		Marks Allotted
	PART-A	
1		1
2	Voltage divider biasing.	1
3	The emitter voltage follows the base voltage. Hence the common collector amplifier is also known as emitter follower.	1
4	Decreases.	1
5	(Triangular) 	1
6	Piezoelectric effect	1
7	The area between the end of ground wave reception and point of first sky wave reception in which no transmission is received is called Silent Zone or Skip Zone.	1
8	$m_a = \frac{V_{max} - V_{min}}{V_{max} + V_{min}}$	1
9	Infinite	1
10	Insulated Gate Bipolar Transistor	1
11	$Y=A \oplus B$ OR $Y= \bar{A}B+A\bar{B}$	1
12	$(1101)_2$	1
13	One	1
14	Y=a*a+b*b	1
15	An Optical fiber communication system uses light as the carrier of information to be transmitted.	1
	PART-B	
16	It is the ratio of change in drain-source voltage (ΔV_{DS}) to the change in gate-source voltage (ΔV_{GS}) at constant drain current (ΔI_D).	1
	$\mu = r_d \, X \, g_m$	1
17	Finding values of 1. $V_{CE.}$ and 2. I_C. 3. End points of dc load line.	1 1
18	 For Voltage divider biasing. (Load R_L is optional).	2

19 The advantages of negative feedback are (Any two each carry one mark) — 2

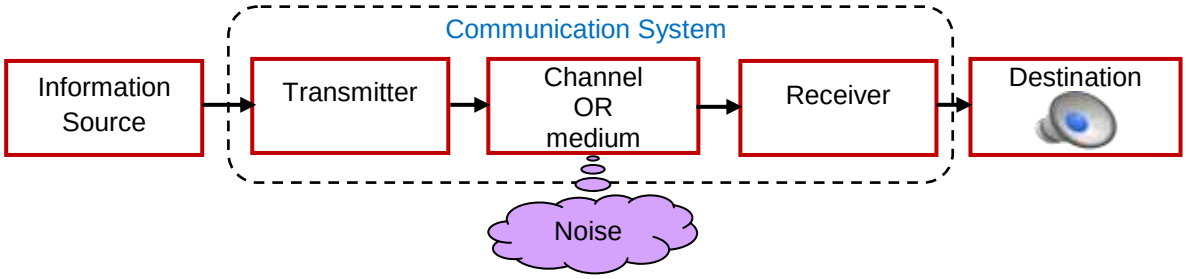
- Reduction in distortion.
- Reduction in noise.
- Stability in gain.
- Increased bandwidth.
- Increase in input impedance.
- Decrease in output impedance.
- Improved frequency response
- More linear operation

20 Characteristics of ideal Op-Amp (Any two each carry one mark) — 2

- The open loop gain is infinity. ($A_v=\infty$).
- Input impedance is Infinity ($Z_i=\infty$).
- Output impedance is zero ($Z_o=0$).
- The band width is infinity (BW=∞)
- Perfect Balance. i.e. The output voltage is zero when both the inputs are equal or zero.
- Characteristics do not drift with temperature.
- Common-mode rejection ratio is infinity.(CMRR=∞).
- Slew rate is infinity.
- Power supply rejection ratio is zero.(PSRR=0)

21
1. The product of the gain and feedback factor or loop gain should be unity. i.e $|A\beta| = 1$ — 1
2. The net phase shift around the loop is 0° or 360° or an integral multiple of 2π radians in other words feedback must be positive. — 1

22



— 2

23 A good Radio receiver should have the following characteristics.

- Selectivity (Any two each carry one mark)
- Sensitivity.
- Stability
- Signal to Noise ratio
- Fidelity

— 2

24 **(Any one)** — 2

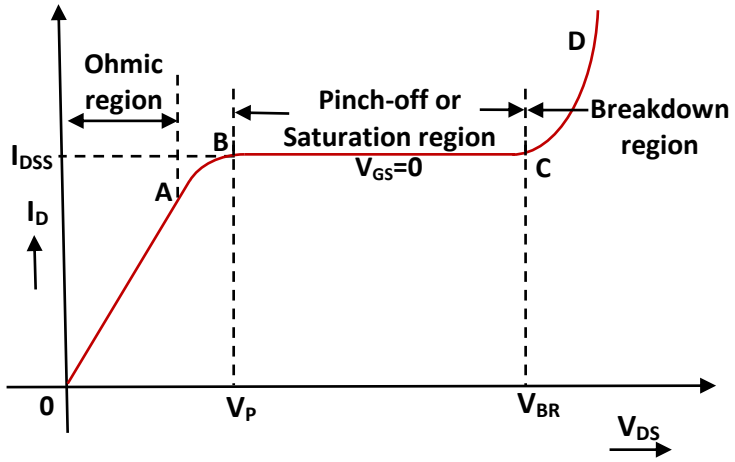
Punch through power diode	Non punch through power diode
In punch through diode width of the depletion layer is almost equal to the width of the drift layer. In punch through power diode strength of the electric field is almost uniform across the drift layer.	In non-punch through diode width of the depletion layer is less than the width of the drift layer. Strength of the electric field is maximum at n^-p^+ junction and decreases as we move towards the n^+ region.

25 Types of protocols used in computer networking are (Any two each carry one mark) 2

- TCP - transmission control protocol
- IP - Internet protocol
- FTP - file transfer protocol
- HTTP - hyper text transfer protocol, etc.

PART-C

26



Characteristic curve is optional.

Ohmic region OA:

This part of the characteristic is linear indicating that for low values of V_{DS}, current varies directly with voltage following Ohm's Law. It means that FET behaves like an ordinary resistor till point A (called knee) is reached. 1

Pinch-off region BC:

It is also known as saturation region or 'amplifier' region. Here, FET operates as a constant-current device because I_D is relatively independent of V_{DS}. It is due to the fact that as V_{DS} increases channel resistance also increases proportionally thereby keeping I_D practically constant at I_{DSS} (drain-source saturation current or Shorted-gate drain current). Drain current in this region is given by Shockley's equation. It is the normal operating region of the FET when used as an amplifier. 2

$$I_D = I_{DSS} [1 - (V_{GS} / V_P)]^2$$

27 *The self-destruction of an unstabilised transistor is known as* ***theral runaway.*** 1

- I_{CBO} collector-base current with emitter open (In CB mode) 1
- I_{CEO} collector emitter current with base open (In CE mode) 1

28 **LAYERS OF IONOSPHERE**

The **D layer** is the lowest, existing at an average height of 70 km, with an average thickness of 10 km. It disappears at night. Because it is the layer farthest from the sun, it has little ionization. It reflects some VLF and LF waves and absorbs MF and HF waves to a certain extent. 1

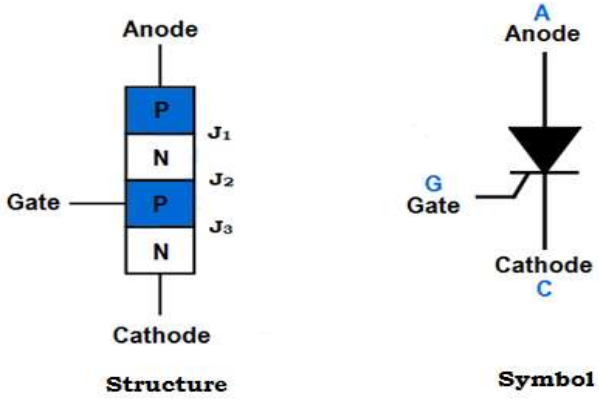
The **E layer** is next in height, existing at about 100 km, with a thickness of perhaps 25 km. Like the D layer, it disappears at night. It reflects almost Very Low frequency signals and low frequency signals and some High 1

frequency (HF) waves in the day time. E layer is called **Kennelly- Heaviside** layer. It is also called as **Sporadic** E- layer

The **F_1 layer** exists at a height of 150 km in daytime and combines with the F_2 layer at nights. Its daytime thickness is about 20 km. Although some HF waves are reflected from it. 1

The **F_2 layer** is by far the most important reflecting medium for high-frequency radio waves. Its approximate thickness can be up to 200 km, and its height ranges from 250 km to 400 km in daytime. At night, it falls to a height of about 300 km, where it combines with the F_1 layer to form **F layer**. F layer is called **Appleton** layer.

29



1

It has four alternating layer and three junctions J_1, J_2, J_3 of N and P type semiconductor material. A thyristor has three terminals such as anode, cathode and gate. The symbol of a thyristor is as shown in fig. 2

30 **Given:** $\alpha = 90^0$, $V_{rms} = 230$ V, $R = 25\ \Omega$

$V_m = \sqrt{2} \times V_{rms} = 325.2$

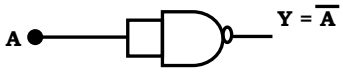
$V_{dc} = \frac{V_m}{\pi}[1 + cos\alpha]$ 1

$= \frac{V_m}{\pi}[1 + \cos(90)] = \frac{V_m}{\pi}[1 + 0] = \frac{325.2}{\pi} \times [1 + 0]$ 1

$V_{dc} = 103.5$ V

$I_{dc} = \frac{V_{dc}}{R} = \frac{103.50}{25} = 4.14$ A 1

31 NAND gate as NOT gate



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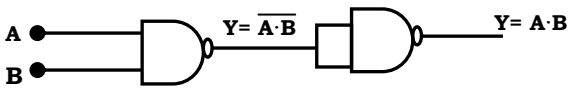
NOT gate can be made out of a NAND gate by connecting its two inputs together.

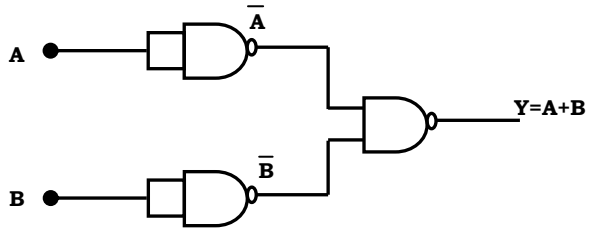
NAND gate as AND gate



1

The use of two NAND gates to produce an AND gate is as shown in fig.

NAND gate as OR gate



1

Fig. shows how OR gate can be made out of the three NAND gates.

32 ***The ways of accessing data by the CPU is called addressing mode.*** 1

Addressing modes are necessary to transfer data, it may be in the memory or in register or supplied with instructions as an immediate value. 2

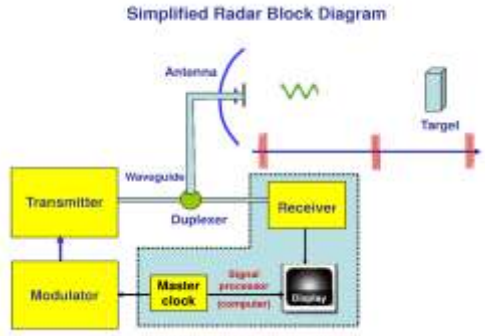
33

```
MOV A, # 01EH ; load 01EH into A                    1
ADD A, # 01CH ; add A to 1CH                        1
MOV R6, A ; now A = A+1CH                           1
NOP ; load A to R6
END
```

34

- **Syntax errors**: These errors occur because of wrongly typed statements, which are not according to the syntax or grammatical rules of the language. 1
- **Logical errors:** These errors occur because of logically incorrect instructions used in the program. 1
- **Runtime errors:** These errors occur when you attempt to run the ambiguous instructions. 1

35



1

Transmitter

The *transmitter* generates the radio-frequency energy in the form of short powerful pulses and sends it to the antenna. 1

Modulator

The *modulator* produces the synchronizing signals in the form of pulses to turn the transmitter on and off.

Duplexer

The duplexer alternately switches the antenna between the transmitter and receiver so that only one antenna need be used. 1

Receiver

The receivers amplify and demodulate the received RF-signals. The receiver provides video signals on the output.

Radar Antenna

Antenna radiates high power signals obtained from the transmitter in to space in a desired direction. It also collects the reflected signal from the target.

Indicator

The indicator uses the received signals from the radar receiver to produce a visual indication of target information.

I

PART-D

36

a) $V_2 = \frac{V_{cc}}{R1+R2} \times R_2$ — 1

$V_2 = \frac{20}{45K+5K} \times 5K$

V_2 =2.0 V

b) $I_E = \frac{V_2 - V_{BE}}{R_E}$ — 1

$\mathbf{I_E} = \frac{2.0-0.7}{1K}$

I_E =1.3mA

$\mathbf{r_e'} = \frac{52\text{ mV}}{I_E} = \frac{52\text{ mV}}{1.3mA}$ **= 40 Ω** — 1

c) $\mathbf{A_v} = -\frac{\mathbf{Z_o}}{\mathbf{r_e'}} = \frac{5K}{40}$ **= -125** — 1

$Z_{in(base)}$=βXr_e'=100X40=4k Ω

d) **Z_{in}**= $R_1 \| R_2 \|$ **$Z_{in(base)}$= 45kΩ‖5 kΩ‖4k Ω = 2.11 kΩ** — 1

e) **Z_o** = $R_C \| R_L$= **10 kΩ‖10 kΩ = 5 kΩ** — 1

37

Given A=200, f_1=100Hz, f_2=20 kHz, β=0.02

$$A_f = \frac{A}{(1+A\beta)}$$ — 1

$$= \frac{200}{(1+200\times0.02)} = \frac{200}{1+4} = \frac{200}{5}$$

A_f= 40 — 1

Lower cut off frequency with negative feedback is

$$f_1' = \frac{f_1}{(1+A\beta)}$$ — 1

$$= \frac{100}{(1+0.02\times200)} = \frac{100}{(1+4)}$$ — 1

f_1' = 20 Hz

Upper cut off frequency with negative feedback is

$$f_2' = f_2(1+A\beta)$$

$$= 20\times10^3(1+0.02\times200)$$

$$= 20\times10^3(1+4)$$

f_2'= **100 kHz** — 1

38

The given circuit is an op-amp inverting amplifier followed by a adder. Therefore output voltage V_{o1} of the op-amp inverter is given by,

$V_{o1} = -\frac{R_f}{R_i} \text{ x } V_i$ — 1

$V_{o1} = -\frac{2.2k}{1k} \text{ x } 300mV$

V_{o1} =-660mV — 1

The given circuit is an inverting adder.

$$V_o = -R_f\left(\frac{V_1}{R_1} + \frac{V_2}{R_2}\right)$$ 1

$$V_o = -47K\left(\frac{-660mV}{10K} + \frac{200mV}{10K}\right)$$ 1

V_o = -2.162V 1

39 $f = \frac{1}{2\pi\sqrt{LC}}$, where $L = L_1 + L_2$ 1

$$1200 \times 10^3 = \frac{1}{2 \times 3.142\sqrt{(20 \times 10^{-6} + L_2) \times 220 \times 10^{-12}}}$$ 1

$$(20 \times 10^{-6} + L_2) = \frac{1}{(1200 \times 10^3 \times 2 \times 3.142)^2 \times 220 \times 10^{-12}}$$ 1

$$(20 \times 10^{-6} + L_2) = \frac{1}{(12 \times 6.284)^2 \times 220 \times 10^{-2}}$$ 1

$L_2 = 80 \times 10^{-6} - 20 \times 10^{-6}$ **$= 60\mu F$** 1

40 The standard equation for FM signal is

$$v = V_c \sin(\omega_c t + m_f \sin\omega_m t)$$

Comparing the above equation, we get

V_c =10 V, $\omega_c = 6 \times 10^8$, m_f =5, ω_m =1250.

Carrier frequency $f_c = \frac{6 \times 10^8}{2\pi}$ = 95.48 MHz. 1

Modulating frequency $f_m = \frac{1250}{2\pi}$ = 199Hz. 1

Modulation index m_f = 5 1

Maximum deviation $\Delta f = m_f \times f_m$ $K_f = \frac{\Delta f}{V_m}$ 1

$= 5 \times 199$

Δf = 995 Hz

Carrier swing CS= $2 \times \Delta f$

= 2x995

= 1990 Hz 1

41

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	**1**	**0**	**0**	x
$\bar{A}B$	x	**0**	**0**	**1**
AB	**1**	**0**	**0**	**1**
$A\bar{B}$	**1**	**0**	**0**	x

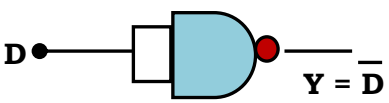
1

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	**1**	**0**	**0**	x
$\bar{A}B$	x	**0**	**0**	**1**
AB	**1**	**0**	**0**	**1**
$A\bar{B}$	**1**	**0**	**0**	x

Octet (first column) Octet (last column)

2

$Y = \bar{D}$ 1



1

II

42 **CB amplifier.** **(Any five each carry one mark)** 5

1. Current gain is less than unity.
2. Voltage gain is very large about 1500.
3. The output impedance is very large (up to 500kΩ) .
4. Very low input impedance (30Ω to 150Ω).
5. Large power gain is up to 30dB.
6. The input and output signals are in phase.

CE amplifier.

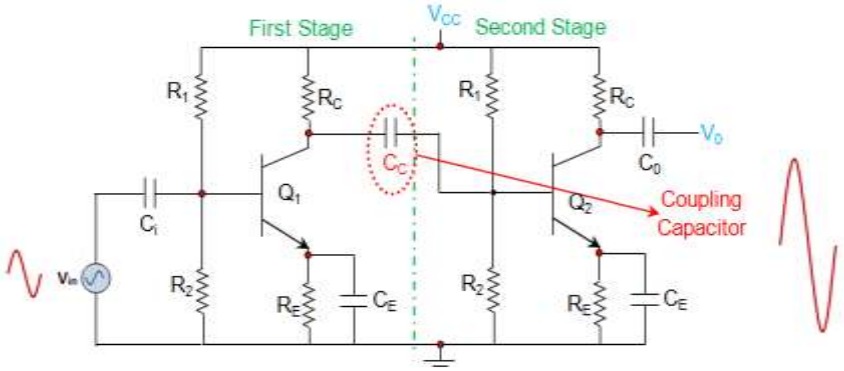
1. The current gain is high.
2. High Voltage gain.
3. Low input impedance.
4. Large output impedance.
5. Power gain is high up to 40dB.
6. The output ac signal has 180° phase shift with the input ac signal.

CC amplifier.

1. The current gain is very large.
2. The Voltage gain is nearly equal to unity.
3. The input impedance is very high (up to 500kΩ).
4. Low output impedance.
5. Power gain is low up to 20dB.
6. The input and output signals are in phase.

Two stage R-C coupled amplifier

43

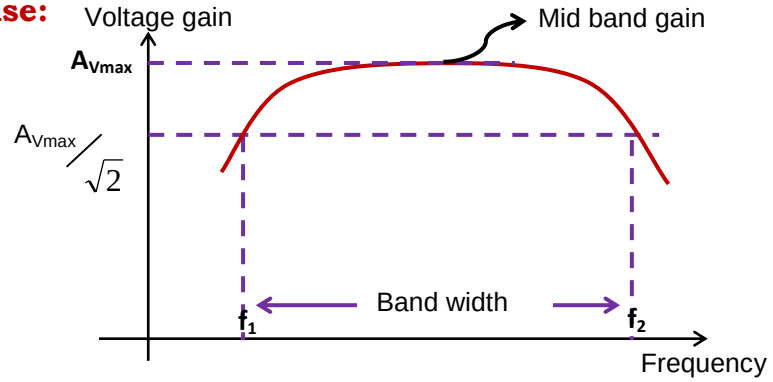


2

Working :

When an AC signal is applied to the input of the first stage, it gets amplified and appears at the output with a phase reversal of 180°. This amplified signal is then fed to the input of the second stage through a coupling capacitor C_C. The coupling capacitor blocks DC and allows AC signals. The second stage further amplifies the signal. The output of the second stage will have a phase reversal of 180° with respect to the input fed to it. The input signal and output signal are in phase since it has been reversed twice. Thus over all voltage gain equals the product of the gain of the individual stages. 2

Frequency response:



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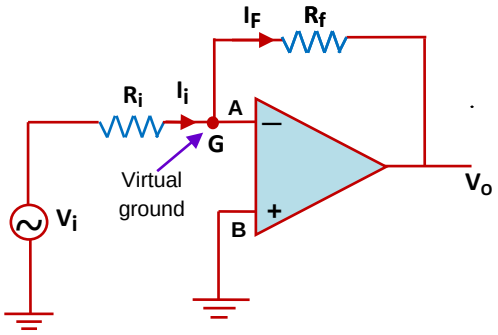
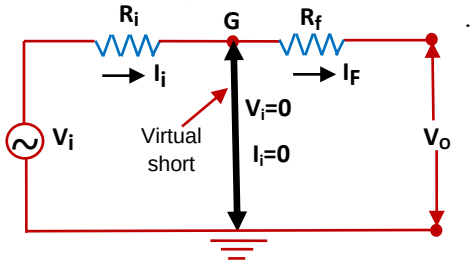
44 (a)





1

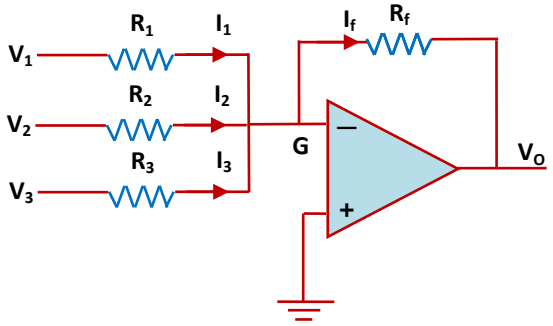
Consider an ideal operational amplifier. The input signal V_i is applied to the inverting terminal of op-amp through a resistor R_i. The non inverting terminal is grounded. R_f is the feedback resistor connected the output back to the inverting input. Since the voltage gain of an ideal op amp is infinite, this forces the voltage between the two inputs must be zero or equal. 1

i.e $V_B - V_A = 0$

$V_B = V_A$

Hence point G in fig is referred to as virtual ground because it is virtually at the ground potential but not physically connected to ground.

(b)



1

The circuit for the op-amp summing amplifier or adder is shown in figure.

Since the input impedance of op-amp is infinite, no current flows through op-amp. If I_1, I_2 and I_3 are the currents through R_1, R_2 and R_3 then Applying KCL we get,

$$I_1 + I_2 + I_3 = I_f$$

$$\frac{V_1 - V_A}{R_1} + \frac{V_2 - V_A}{R_2} + \frac{V_3 - V_A}{R_3} = \frac{V_A - V_O}{R_f}$$ 1

As $V_G = 0$,

$$\frac{V_1 - 0}{R_1} + \frac{V_2 - 0}{R_2} + \frac{V_3 - 0}{R_3} = \frac{0 - V_O}{R_f}$$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = \frac{-V_O}{R_f}$$

$$V_O = -R_f\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)$$ 1

If $R_1 = R_2 = R_3 = R_f = R$,

$$\mathbf{V_o = -(V_1 + V_2 + V_3)}$$

Thus the output voltage is the negative sum of input voltages. So under this condition summing amplifier is also called **op-amp inverting adder.**

45

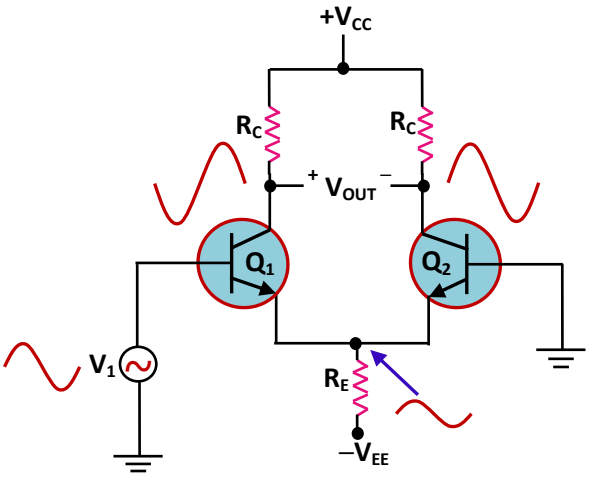


Fig (a)

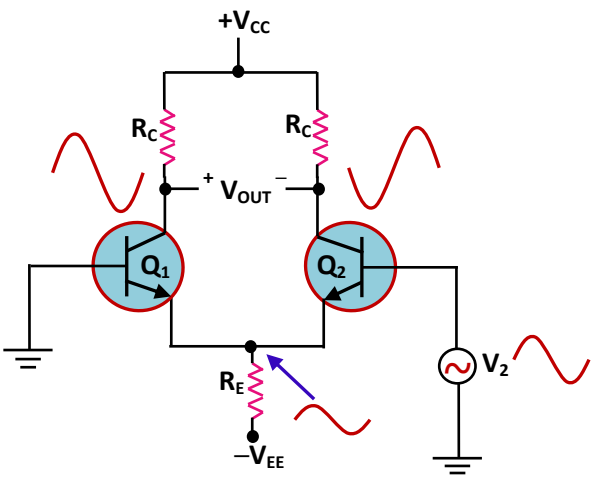


Fig (b)

2

The circuit of **Dual input balanced output differential amplifier** is as shown in fig.V_1 and V_2 are the two inputs, applied to the bases of Q_1 and Q_2 transistors. The output voltage is measured between the two collectors which are at same dc potentials.

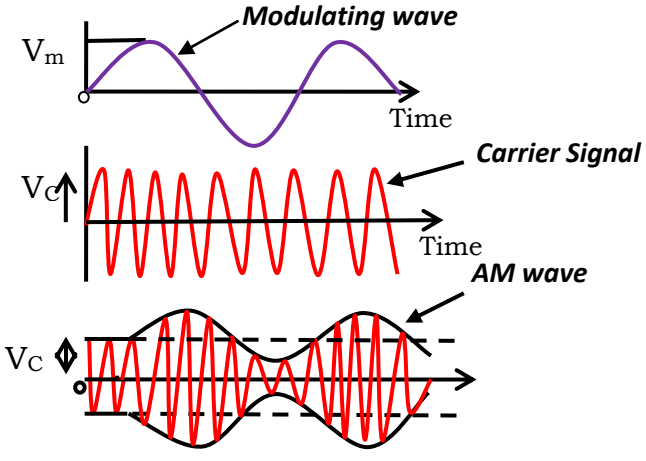
Working:

When an ac input signal V_1 is applied to the base of transistor Q_1 and base of transistor Q_2 is grounded as shown in Fig (a). The transistor Q_1 will act as a common emitter amplifier. Hence an amplified inverted signal appears at collector of Q_1. As a common collector amplifier, the signal appears on the emitter of Q_1 in phase with the input. Since the emitters of Q_1 and Q_2 are common, the emitter signal $V_1/2$ becomes input to Q_2.Therefore, transistor Q_2 functions as a common base amplifier and amplified signal appears on collector of Q_2 in phase with input signal V_1. 1

When an ac input signal V_2 is applied to the base of transistor Q_2 and base of transistor Q_1 is grounded as shown in Fig (b). The transistor Q_2 works as common emitter amplifier while transistor Q_1 works as common base amplifier. Therefore an inverted amplified signal appears at the collector Q_2 and non inverted amplified signal appears at the collector of Q_1. 1

When the both input signal V_1 and V_2 are simultaneously applied using super position theorem the resultant output voltage is given by $V_O = A_d(V_1 \sim V_2)$.Where A_d voltage gain of differential amplifier. 1

46 *When the amplitude of high frequency carrier wave is changed in accordance with the instantaneous voltage of the modulating signal, keeping the frequency and phase of carrier constant is known as Amplitude modulation.* 1



Analysis of amplitude modulated wave.

Let the instantaneous voltage of modulating signal is

$$v_m = V_m \text{ Sin } \omega_m t \quad \ldots\ldots \quad (1)$$ 1

Where V_m is the amplitude of the modulating signal and $\omega_m = 2\pi f_m$ is the angular frequency.

Let the instantaneous voltage of the carrier signal be

$$v_c = V_c \text{ Sin } \omega_m t \quad \ldots\ldots \quad (2)$$ 1

Where V_c is the amplitude of the carrier signal and $\omega_c = 2\pi f_c$ is the angular carrier frequency. The phase angle is ignored in both expressions since these do not change during amplitude modulation.

In amplitude modulation the amplitude of the carrier signal varies in accordance with the modulating value v_m of the signal amplitude.

If '**A**' is the amplitude of the modulated wave then we have,

$$A = V_c + v_m$$ 1

$$A = V_c + V_m \text{ Sin } \omega_m t$$

$$A = \frac{V_c}{V_c} [1 + V_m \text{ Sin } \omega_m t]$$

$$A = V_c \ [1 + m_a \text{ Sin } \omega_m t] \ldots\ldots\ldots\ldots (3)$$

Where $m_a = \frac{V_m}{V_c}$ called modulation index or modulation factor or depth of modulation of AM wave.

As the frequency of the carrier is unaltered the instantaneous voltage of resulting amplitude modulated wave is given by

$$v_{AM} = A \text{ Sin} \omega_c t \quad \ldots\ldots\ldots\ldots\ldots (4)$$

Substituting equation (3) in (4) we get

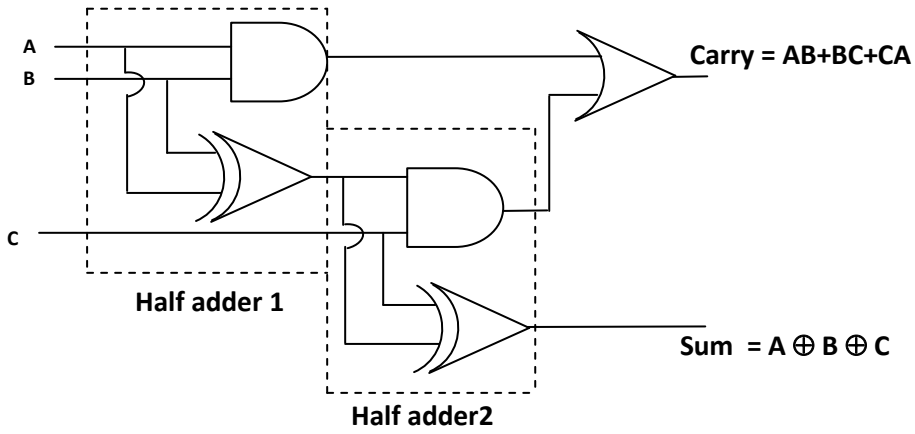
$$v_{AM} = V_c [1 + m_a \text{ Sin } \omega_m t] \text{ Sin} \omega_c t \quad \ldots\ldots\ldots\ldots\ldots (4)$$ 1

$$v_{AM} = V_c \text{ Sin } \omega_c t + \frac{m_a V_c}{2} \text{ Cos } (\omega_c - \omega_m)t - \frac{m_a V_c}{2} \text{ Cos } (\omega_c + \omega_m)t$$

47

The combinational logic circuit that performs the addition of 3 bits is called a full adder. A full adder accepts 3 bits on its input and produce a SUM bit and a CARRY bit on its output. 1

Full adder using two input XOR gate and AND gates



1

Working:

(Truth table is optional)

A	B	C	CARRY	SUM
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
1	0	0	0	1
0	1	1	1	0
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

3

Case (1)

When Input A = 0, B = 0 and C = 0

Full adder response: SUM = 0 and CARRY = 0.

Case (2)

When A = 0, B = 0 and C = 1

Full adder response: SUM = 1 and CARRY = 0.

Case (3)

When A = 0, B = 1 and C = 0

Full adder response: SUM = 1 and CARRY = 0.

Case (4)

When A = 1, B = 0 and C = 0

Full adder response: SUM = 1 and CARRY = 0.

Case (5)

When A = 0, B = 1 and C = 1

Full adder response: SUM = 0 and CARRY = 1.

Case (6)

When A = 1, B = 0 and C = 1

Full adder response: SUM = 0 and CARRY = 1.

Case (7)

When A = 1, B = 1 and C = 0

Full adder response: SUM = 0 and CARRY = 1.

Case (8)

When A = 1, B = 1 and C = 1

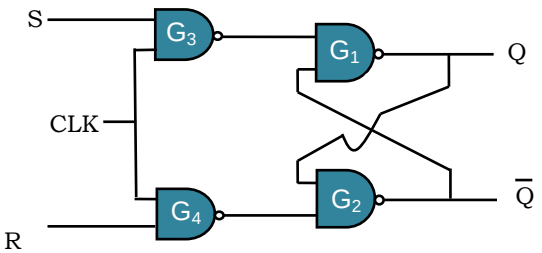
Full adder response: SUM = 1 and CARRY = 1.

48 (a)

- SR flip flop. (Any two each carry one mark)
- D flip flop.
- JK flip flop.
- Master Slave JK flip flop.
- T flip flop.

2

(b)



1

Figure shows the clocked SR flip flop. This flip flop can SET or RESET in synchronizing with clock. In the truth table the output is shown as Q_{n+1} this is because it must be considered two different instant. The output before CLK Q_n and the output Q_{n+1} after the CLK.

Working:

When the CLK is LOW. i.e CLK=0 irrespective of the values of R and S the output $Q_{n+1}=Q_n$ i.e the output remains at the previous state. With CLK=1 we have four possible cases. 1

Case (1) When S=0 and R=0, both inputs are low, the output does not change and it remains in the previous state. (HOLD)

Case (2) When S=1 and R=0, R input is low and S input is high, the output of flip-flop is SET (Q=1 and $\overline{Q}$= 0)

Case (3) When S=0 and R=1, R input is high and S input is low, the output of flip-flop is RESET (Q=0 and $\overline{Q}$=1)

Case (4) When S=1 and R=1, inputs both are high, the output is forbidden. This is called INVALID condition

Truth Table 1

Inputs			output	State
CLK	S	R	Q_{n+1}	
0	x	x	Q_n	HOLD
1	0	0	Q_n	HOLD
1	1	0	1	SET
1	0	1	0	RESET
1	1	1	1(?)	INVALID

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```
#include <stdio.h>                                          1
void main()
{
int n, i, sum=0;                                            1
printf("Enter the value of n\n");
scanf("%d", &n);                                            1
i=1;
while (i<=n)                                                1
{
Sum=sum+i;
i++;
}                                                           1
Printf(*sum=%d\n", sum);
}
```